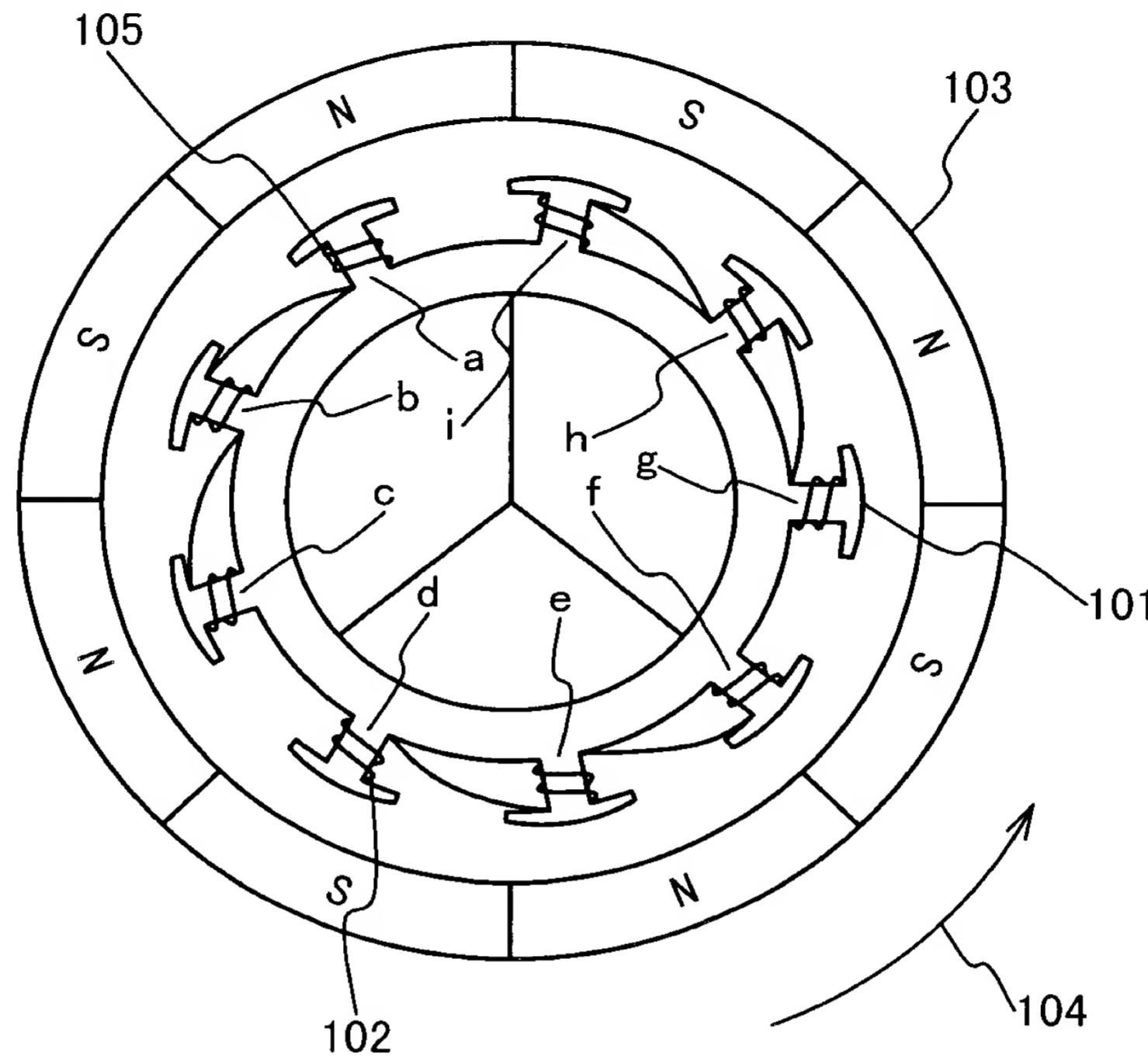


# Fig. 1A PRIOR ART



# Fig. 1B PRIOR ART

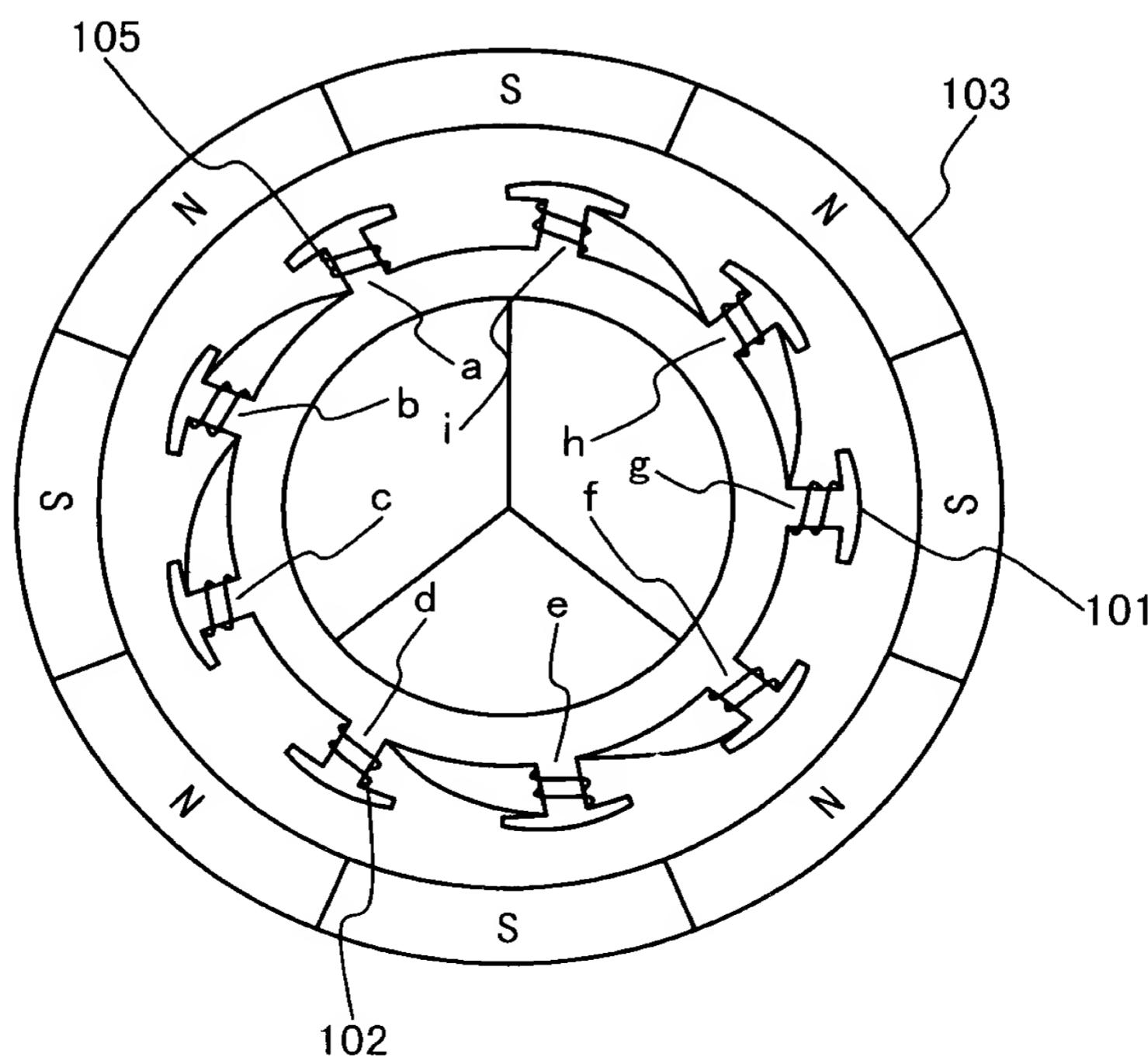


Fig. 2 PRIORITY ART

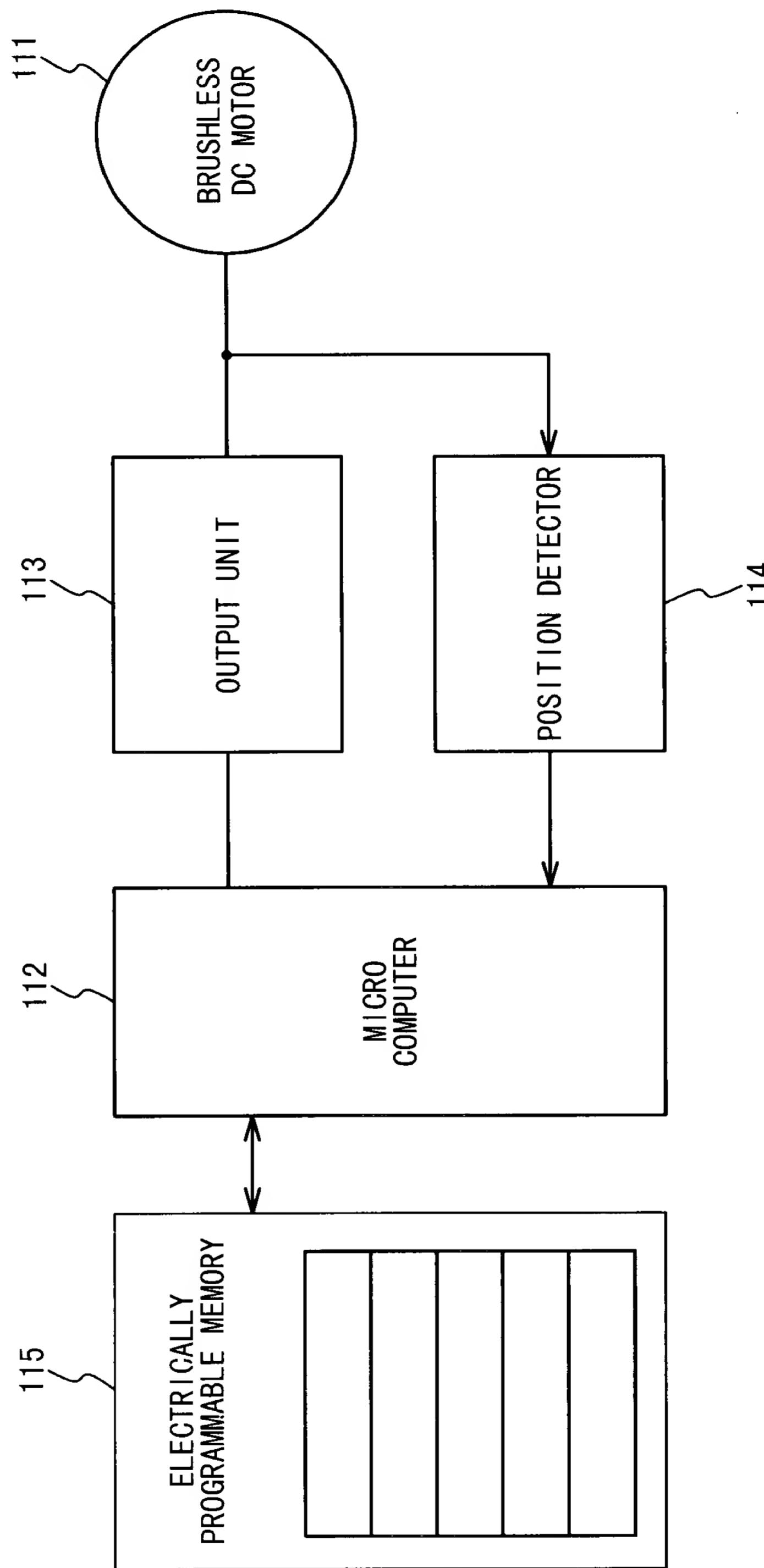


Fig. 3A PRIOR ART

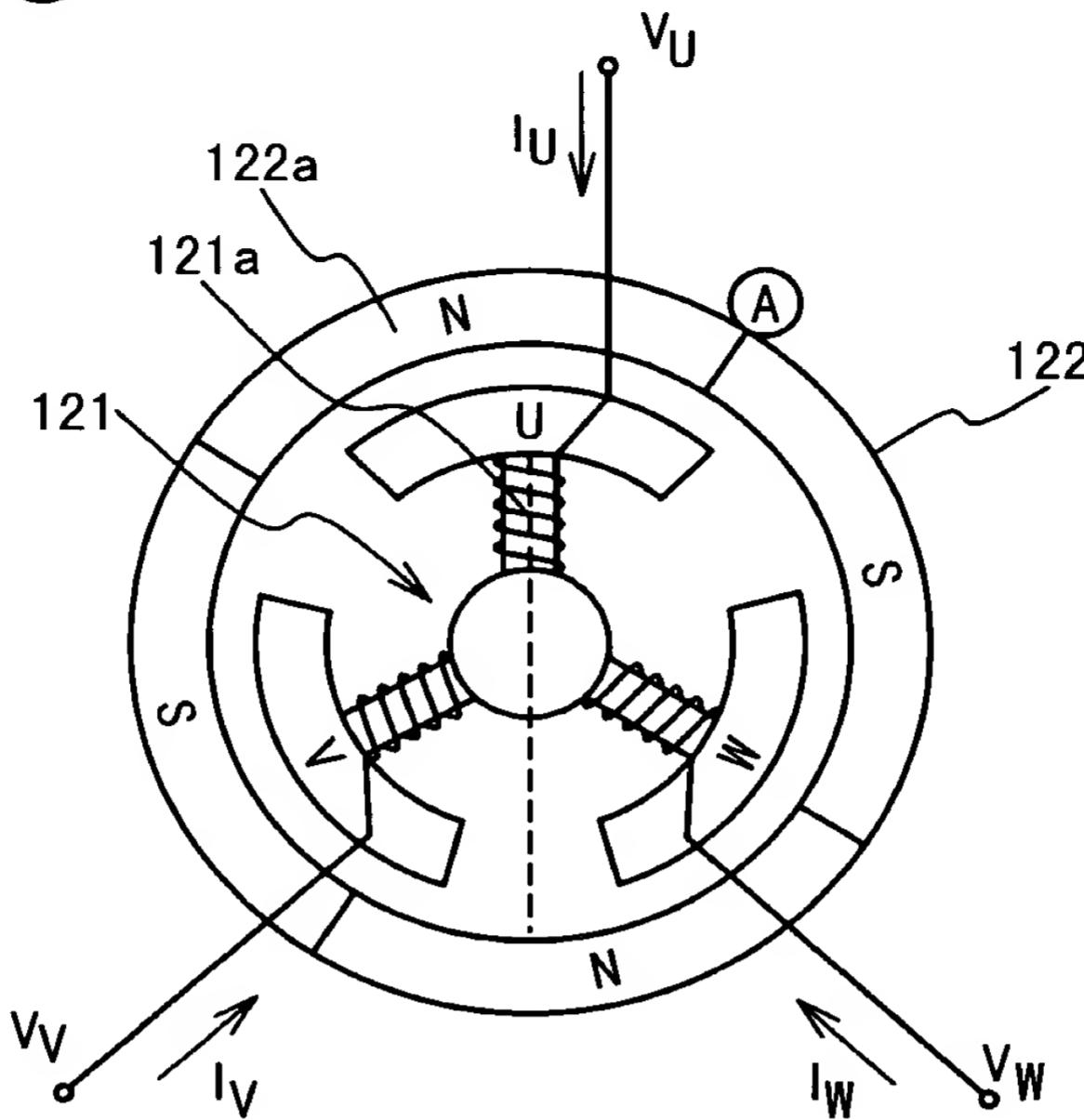


Fig. 3B PRIOR ART

TIMING	(1)	(2)	(3)	(4)	(5)	(6)
U PHASE DRIVE VOLTAGE $V_U$	$V_{CC}$	$V_{CC}$	N. C.	GND	GND	N. C.
V PHASE DRIVE VOLTAGE $V_V$	GND	N. C.	$V_{CC}$	$V_{CC}$	N. C.	GND
W PHASE DRIVE VOLTAGE $V_W$	N. C.	GND	GND	N. C.	$V_{CC}$	$V_{CC}$

Fig. 3C PRIOR ART

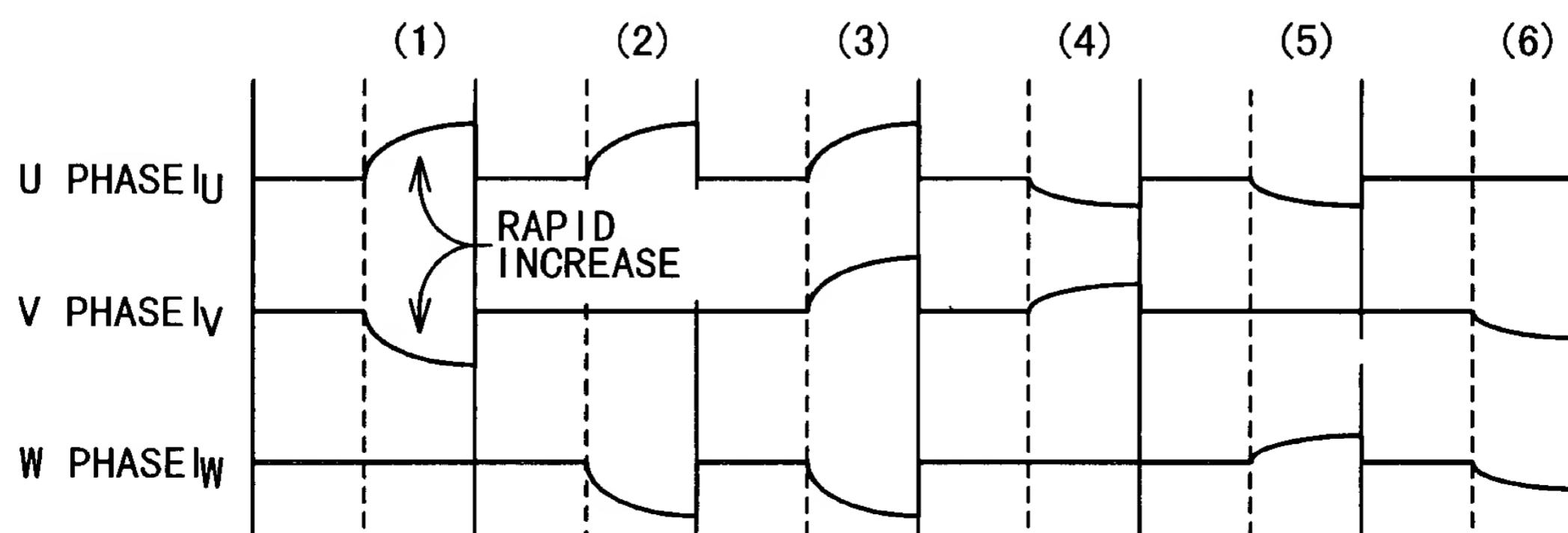


Fig. 4

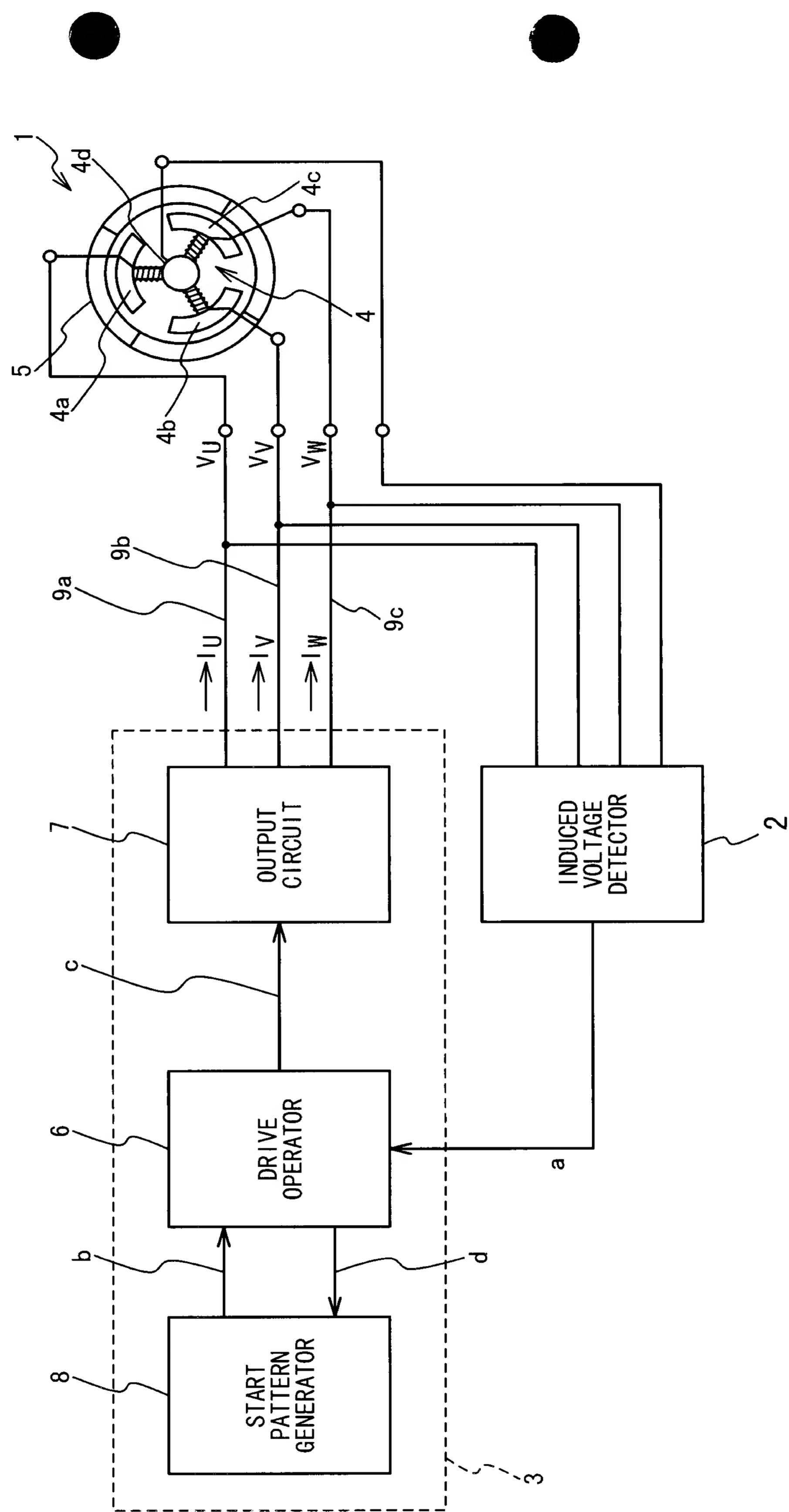


Fig. 5

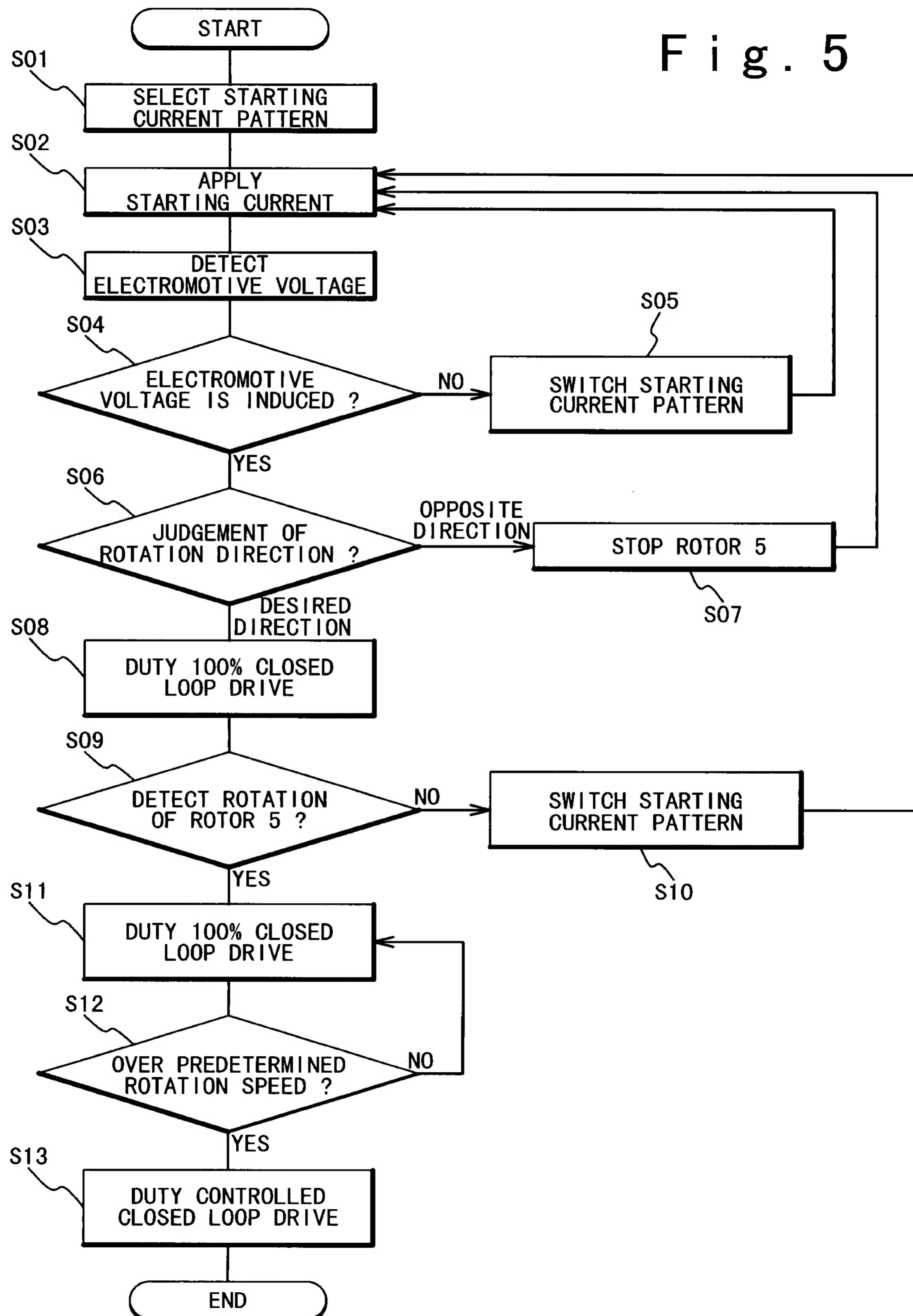


Fig. 6

STARTING CURRENT PATTERN	STARTING CURRENT	U PHASE LINE $g_a$	V PHASE LINE $g_b$	W PHASE LINE $g_c$
PATTERN 1	V→U	GND	$V_{cc}$	NC
PATTERN 2	V→W	NC	$V_{cc}$	GND
PATTERN 3	U→W	$V_{cc}$	NC	GND
PATTERN 4	U→V	$V_{cc}$	GND	NC
PATTERN 5	W→V	NC	GND	$V_{cc}$
PATTERN 6	W→U	GND	NC	$V_{cc}$

Fig. 7

